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08/903,453	07/29/1997	LEONARD FORBES	303.378US1	2271

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EXAMINER
ECKERT II, GEORGE C

ART UNIT	PAPER NUMBER
2815	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 08/903,453	Applicant(s) Forbes et al.
	Examiner George C. Eckert II	Art Unit 2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Apr 21, 2003* .

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *2, 3, 24-28, 41-48, 50-52, and 65-68* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *2, 3, 24-28, 41-48, 50-52, and 65-68* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 42
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Amendment

1. Applicant's response dated April 21, 2003 has been entered of record. Claims 2, 3, 24-28, 41-48, 50-52 and 65-68 are pending.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321© may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 2, 3, 24-28, 41-48, 50-52 and 65-68 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 11-18, 23, 24, 28, 32-37, 40, 48, 62, 67 and 69 of co-pending Application No. 08/902,843. Although the conflicting claims are not identical, they are not patentably distinct from each other because the present invention and co-pending Application no. 08/902,843 disclose a transistor having:

a source and a drain separated by a channel supported by a semiconductor substrate;

a floating gate formed between the source and the drain above the channel and separated by an insulative amorphous carburized silicon layer;

a control gate formed adjacent to and insulated from the floating gate;

wherein the transistor is part of a memory cell comprising a capacitor.

Further, stacked capacitors are well known and widely used in memory devices.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 U.S.C. § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 2, 3, 24-28, 41-48, 50-52 and 65-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakata et al., *Amorphous silicon/amorphous silicon carbide heterojunctions applied to memory device structures*, Electronics Letters, April 28, 1994, Vol. 30, No. 9 (of record), in view of JP 8-255878 to Sugita et al. (of record) and Burns et al., *Principles of Electronic Circuits* (of record).

With regard to claims 2, 3, 24, 45, 46, 48, 50, 52, and 68, Sakata et al. teach in figure 1 the formation of an insulative layer of amorphous silicon carbide, shown as the a-SiC:H (graded) layer, formed on top of a substrate which is crystalline silicon (c-Si) that can be p-type (see *Sample Preparation*);

a floating gate formed of amorphous silicon, shown as the a-Si:H layer, formed above the amorphous silicon carbide insulator,

a second insulative layer of amorphous silicon carbide, shown as the a-SiC:H layer, formed above the a-Si:H floating gate, and

a control gate shown as metal in figure 1 and later taught as aluminum (see *Sample Preparation*).

And though Sakata et al. teach that the above structure "can be applied to floating-gate memory devices[,]" Sakata et al. do not teach the structure further comprising a source region, a drain region, or a channel region therebetween. However, such regions are taught by Sugita et al. Specifically, Sugita et al. teach, with reference to figure 1, a floating gate memory device comprising:

an N+ type source region 2 and an N+ type drain region 3 (see page 11, paragraph 0032 of the translated reference which states that the source and drains 2 and 3 are n+ type);

the source and drain regions formed in a p-type silicon substrate (see page 2 of the translated reference which lists the reference numerals and corresponding elements and shows that numeral 1 represents a p-type silicon substrate);

a channel region between the source and drain regions in the substrate (though the channel region is not numbered, it is inherent that there exists a channel region between the source and drain of a transistor, see *Principles of Electronic Circuits*, pp. 382-83 shows an n+ source and an n+ drain in a p-type substrate and refers to the device as one comprising an "n-channel");

a floating gate 6 (see page 3 of the translated reference and the list of elements which labels numeral 6 as a polysilicon floating gate) which is formed above and insulated from the substrate;

a control gate 8 formed above the floating gate and separated from the floating gate by a dielectric layer 7 (again, see the list of elements on page 3 of Sugita et al. where element 8 is labeled a control gate and element 7 is listed as SiO_2, a known, inherent insulator).

Sakata et al., Sugita et al. and Burns et al. are combinable because they are from the same field of endeavor, which field is the formation of floating gate devices. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form a source region, drain region and channel region in the device of Sakata et al. The motivation for doing so is that the source, drain and channel regions allow individual floating gate devices to be formed in an array. That is, by forming source and drain regions having the floating gate stack therebetween, a plurality of floating gate devices can be formed in one substrate and yet be individually written and erased by the use of the source, drain and channel regions. The use of the source/drain/channel regions for such programming is well known in the art. For example, Burns et al. explicitly teach such programming steps in the paragraph bridging pages 382-83. Furthermore, Sugita et al. generally teach this integration concept in paragraphs 0001 - 0005 of the translated reference. Therefore, it would have been obvious to combine Sakata et al. with Sugita et al. and Burns et al. to obtain the invention of claims 2, 3, 24-28, 41-48, 50-52, & 65-68.

Regarding the use of polysilicon as the material for the control gate, Sakata et al. indicate that the control gate is formed of aluminum while Sugita et al. are silent as to the material for their control gate. However, Burns et al. teach on page 382 that control gates (or, as there labeled, select gates) are typically formed of polysilicon. Even beyond the teaching of Burns et al., the use of polysilicon as a control gate is considered well known in the art. There are several advantages of using polysilicon as a control gate, for example, polysilicon can be doped to a low resistivity and is able to withstand higher temperatures so that it is unaffected during subsequent annealing steps. As such, it is considered obvious to form the control gate of Sakata et al. from polysilicon.

As to the method of formation of the insulation layer between the floating gate and the substrate from silicon carbide, Sakata et al. teach or in the alternative make obvious such a structure. The limitation that the amorphous carburized silicon is *grown* on the substrate is taught or in the alternative obvious over Sakata et al. In support of the process term *grown*, it is noted that applicant's *growth* method is a deposition (specification p. 6, lines 3-4). Sakata et al. also teach a deposition method (see *Sample preparation*). As such, Sakata et al.'s deposition process anticipates the growth process limitation as instantly claimed.

In the alternative, and with further regard to the limitation where the *growth* process is further limited to be a microwave PECVD, limitations in the instant claims as to the process by which the final product is achieved do not distinguish over that taught by Sakata et al. That is, such limitations are product by process limitations. Note that a "product by process" claim or limitation is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ

15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that, once a product appearing to be substantially identical is found and a rejection is made, the burden shifts to the applicant to show an unobvious difference based on the claimed process steps. MPEP §2113. Instantly, because no evidence was proffered by applicant as to patentability based on the added process limitations, the burden remains with applicant to do so.

4. Claims 2, 3, 24-28, 41, 45, 46, 50, 65 and 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lott et al., *Charge Storage in InAlAs/InGaAs/InP Floating Gate Heterostructures* (from IDS, Paper #40) in view of Sakata et al., *Amorphous silicon/amorphous silicon carbide heterojunctions applied to memory device structures* (of record).

Lott et al. teach in figure 2 a floating gate device having an N+ source and an N+ drain separated by a channel ("sense channel") which source/drain and channel form a substrate, a gate supported by the substrate and extending between the source and drain above the channel; and a barrier on the channel and between the channel and the gate. Lott et al. also teach in figure 2 a

floating gate and control gate insulated from each other. However, Lott et al. do not teach that the barrier layer is an insulative amorphous layer of carburized silicon grown on the channel or that the substrate is p-type Si.

Sakata et al. teach, with reference to figure 1, a device in which an amorphous layer of carburized silicon (a-SiC:H) is formed directly on a substrate made of silicon (c-Si). Sakata et al. further teach that the substrate may be p-type (page 688, col. 2, under *Sample Preparation*).

As to the method of formation of the insulation layer between the floating gate and the substrate from silicon carbide, Sakata et al. teach or in the alternative make obvious such a structure. The limitation that the amorphous carburized silicon is *grown* on the substrate is taught or in the alternative obvious over Sakata et al. In support of the process term *grown*, it is noted that applicant's *growth* method is a deposition (specification p. 6, lines 3-4). Sakata et al. also teach a deposition method (see *Sample preparation*). As such, Sakata et al.'s deposition process anticipates the growth process limitation as instantly claimed.

In the alternative, and with further regard to the limitation where the *growth* process is further limited to be a microwave PECVD, limitations in the instant claims as to the process by which the final product is achieved do not distinguish over that taught by Sakata et al. That is, such limitations are product by process limitations. Note that a "product by process" claim or limitation is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209

USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that, once a product appearing to be substantially identical is found and a rejection is made, the burden shifts to the applicant to show an unobvious difference based on the claimed process steps. MPEP §2113. Instantly, because no evidence was proffered by applicant as to patentability based on the added process limitations, the burden remains with applicant to do so.

Lott et al. and Sakata et al. are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the floating gate memory device of Lott et al. using the silicon based materials taught by Sakata et al., specifically the amorphous silicon carbide insulating layer on the silicon substrate. The motivation for doing so, as is taught by Sakata et al., is that devices using a III-V heterojunction suffer excessive leakage current which is reduced by using the silicon based materials. Therefore, it would have been obvious to combine Lott et al. with Sakata et al. to obtain the invention of claims 2, 3, 24, 45, 46, 50, 52 and 68.

5. Claims 42, 43, 47, 48, 51, 52, 66 and 67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lott et al. in view of Sakata et al. and Burns et al. (of record). Lott et al. and

Sakata et al. teach the structure of the instant claims but did not teach that control gate was made of polysilicon. Burns et al. teach on page 382 that control gates (or, as there labeled, select gates) are typically formed of polysilicon.

Lott et al. and Sakata et al. are combinable with Burns et al. because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to form the device of Lott et al. and Sakata et al. having a polysilicon control gate electrode as taught by Burns et al. The motivation for doing so is that there are several advantages of using polysilicon as a control gate, for example, polysilicon can be doped to a low resistivity and is able to withstand higher temperatures so that it is unaffected during subsequent annealing steps. As such, it is considered obvious to form the control gate of Lott et al. and Sakata et al. from polysilicon. Therefore, it would have been obvious to combine Lott et al., Sakata et al. and Burns et al. to obtain claims 42, 43, 47, 48, 51, 52, 66 and 67.

Response to Arguments

6. Applicant's arguments filed April 21, 2003 have been fully considered but they are not persuasive. Applicant begins arguments by stating the requirements for establishing a *prima facie* case of obviousness, citing *Vaeck* and *Lee* which require that the suggestion or motivation to combine references "be based on objective evidence of record." Applicant first argues that the obviousness rejection over Sakata, Sugita and Burns must fail as the requirements of *Vaeck* and

Lee are not met - that the rejection lacks any objective evidence which suggests or motivates the combination of the references. These arguments are not persuasive.

The motivation cited in the previous Office action and repeated above is that source, drain and channel regions allow individual floating gate devices to be formed in an array. Applicant argues that there is no evidence of record which supports the above stated motivation. This simply is not true. While it is conceded that Sakata is silent as to the words source, drain and array, it must be acknowledged that Sakata does state, in no uncertain terms: "In this Letter we propose and experimentally confirm that the HJ structure shown in Fig. 1 can be applied to **floating-gate memory devices." (Emphasis added)**. It is known in the art, as taught by both Sugita and Burns, that a floating gate memory device comprises not only a floating gate and a control gate, but also a source and a drain. It is also known in the art that a floating gate memory device is formed having a source and a drain so that individual memory cells may be formed in an array wherein each cell may be programmed individually. This was made clear by the teaching of Burns, cited in the previous rejection and repeated above. As such, the requirement of *Vaeck* and *Lee* are met - objective evidence does support the stated motivation.

Applicant also argues the rejection of the claimed polysilicon control gate in that there is no supporting objective evidence as to the motivation cited. The teaching of a polysilicon control gate comes from Burns. And while Burns is silent as to why the control gate should be formed of polysilicon, the use of polysilicon is ubiquitous in the art. The motivation for using polysilicon, as stated in the rejection, is that polysilicon may be doped to a low resistivity. Such use of

polysilicon is well known in the art. For example, page 281 of W. Scot Ruska's *Microelectronic Processing* is included which teaches this benefit of polysilicon. Specifically, polysilicon can be doped to a low resistivity and can serve as a useful conductor in a number of applications. As such, argument as to the motivation for use of polysilicon as the control gate is not persuasive.

Applicant next argues that evidence in the record also negates the rejection over Sakata in view of Sugita and Burns. That is, while Sakata teaches that the HJ device is programmed by electron injection into the a-Si:H layer and erased by hole injection into the same layer to recombine with the electrons, Burns teaches that a typical floating gate device is not erased using holes. Therefore, according to Applicant, the different operations of the two references denies their combination. However, there are at least two reasons why this argument is not persuasive.

First, it is not dispositive that Burns does not mention holes in the erase process of a floating gate device. Especially in light of the teachings of Wolf. Specifically, Wolf, on pages 625-26 (of record) explains the program and erase mechanisms of a floating gate device. There, Wolf teaches that, like the devices of Sakata, Sugita and Burns, a floating gate device is programmed by electrons stored on the floating gate by the creation of hot electrons near the drain which electrons traverse the oxide (gate insulator) and charge the floating gate. Wolf also teaches that to erase the cell, as in the teaching of Burns, UV light is applied to the gate. However, unlike Burns which only states that the UV light imparts energy to the electrons which allows them to escape, Wolf gives a better explanation of the mechanism. Specifically, Wolf teaches that "the UV light creates electron-hole pairs in the SiO_2, providing a discharge path for

the charged floating gate." As such, electrons and holes are both involved in the erase process of a floating gate device.

Second, regardless of the mechanism of charge storage or erasure, the combination of the references does not change the principle of operation of either device nor negate the combination itself. That is, Sugita was relied on merely for teaching the use of source, drain and channel regions. The addition of these regions in the device of Sakata will not alter the manner in which electrons are stored or erased. Rather, as made clear in the rejection, the use of source, drain and channel regions simply facilitates the use of the HJ structure in an array. Specifically, a floating gate device is formed such that the floating gate is located between a source and drain, with the channel therebetween. By this arrangement, voltage may be applied to selected sources and drains to charge or program an individual cell. This is well known in the art and taught by Burns, as well as by Ng and Wolf. For example and as pointed out in the rejection, Burns teaches on page 383 that an individual cell is programmed by application of voltage to form a channel region between a source and drain, and from that channel electrons are excited and gain enough energy to charge the floating gate. Such use of a source and drain to supply electrons does not alter the principle of operation of the Sakata device.

Furthermore, the connection of a standard floating gate cell is shown by Burns in figure 9.10(a) on page 382 (of record). There, an individual cell is shown in a typical array configuration, where the word line is connected to the control gate, the bit line connected to the drain, and the source is grounded. It is by the use of a source, drain and channel, such as that

taught by Sugita, that the HJ structure of Sakata can be arranged and used in an array, which array is then used to store data. These teachings - the use of a source, drain and channel regions - do not alter the principle of operation of Sakata's HJ device. Rather, with the use of a source, drain and channel, a great number of floating gate cells, wherein each cell stores one bit of data by individual charging or discharging, can be arranged in rows and columns to thereby store a great deal of data. Such is taught by Burns (p. 383, last para.).

Applicant next argues that the prior submission of text book pages from Sze and Streetman still support the position that source and drains cannot be used in the device of Sakata. Specifically, because Sze and Streetman both teach heterojunction devices which do not use source and drains, the heterojunction structure of Sakata must also exclude sources and drains. This is not persuasive. There are many devices in the industry that do not use sources and drains. Many of these devices are formed in bulk silicon, for example neither the elemental p-n diode nor the bipolar transistor are formed with sources or drains. However, it is not because sources and drains cannot be formed in the material, it is because those devices do not have use for a source or drain. Similarly, the devices taught by Sze and Streetman have no need for a source or drain and thus do not form either. However, this does not support applicant's conclusion that a device formed having a heterojunction cannot be formed having a source and drain. Motivation was established for forming the device of Sakata with a source and drain. That other devices exist without a source and drain is not dispositive to that conclusion and the argument is not persuasive.

Applicant next repeats arguments from a previous response regarding the teaching of Qian and now adds that the burden lies with the Patent Office to establish a *prima facie* case of obviousness. The prior response to the argument regarding Qian will not be repeated as it has not changed nor need be amended based on the instant argument. As to the additional argument by applicant regarding the burden on the Office, such burden has been met as pointed out in the above rejection and supporting arguments.

The next argument as to Sakata in view of Sugita and Burns is also taken from previous correspondence. Specifically, applicant argues that the teaching of Capasso, Lott-1 and Lott-2 negate the rejection based on a more likely final structure should Sakata be configured with a source and drain. These arguments were addressed in the previous Office action and will not be repeated here. (Paper No. 41, pages 11-15). In all, these arguments are not persuasive.

Lastly, applicant again argues that objective evidence has not been cited to support the instant rejection. As pointed out above however, objective evidence does exist of record and was cited in the rejection. As such, the argument is not persuasive and the rejection is maintained.

Applicant next turns to the rejection over Lott-2 in view of Sakata and argues that the motivation cited is not applicable to the combination and, even if it is applicable, it is a suggestion to replace the entire structure of Sakata for that of Lott-2 as opposed to modifying Lott-2. These arguments are not persuasvie.

Applicant argues that the motivation cited by Sakata, that the silicon based gate structure has low leakage current, is not applicable to all III-V devices such as that of Lott-2. However,

the motivation established by Sakata is that the use of the silicon based gate structure will reduce leakage current. It is not limited to replacing only the structure of Capasso but merely mentions that it is an improvement over Capasso. The motivation provided is sufficient to combine the teaching with Lott-2.

As to what structure of Sakata goes where in Lott-2, contrary to applicant's assertion, Sakata does not give a suggestion of wholesale replacement of its device (which is to say a memory device which does not have a source and drain) for that of Lott-2 or even Capasso for that matter. Rather, Sakata teaches a stacked structure by which charge may be stored. Lott-2 similarly teaches stacked layers, here comprising the gate and floating gate with the layers of InAlAs therebetween. The modification to Lott-2 is the replacement of one stack for the other, essentially the fabrication of the device of Lott-2 in silicon using the gate stack of Sakata. Applicant would instead rely on Sakata's lack of teaching a source/drain as evidence they do not exist and would not exist in the modified device of Lott-2. However, this again ignores the fundamental nature of sources and drains in memory devices. As discussed above and as known in the art, a source and drain make the memory stack of Sakata, the stack of Lott-2, the stack of Capasso, the stack of Sugita, and the stack of Burns useful in an array. Arguments to the contrary ignore the express direction of Sakata that the device may be applied to floating gate memory devices and that such memory devices have sources and drains. In all, the arguments are not persuasive and the rejection is maintained.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (703) 305-2752.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Eddie Lee can be reached on (703) 308-1690. The fax number is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

GCE
July 11, 2003

GEORGE ECKERT
PRIMARY EXAMINER